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SCULLY SCOTT MURPHY & PRESSER, PC
400 GARDEN CITY PLAZA
SUITE 300
GARDEN CITY, NY 11530

EXAMINER	
DUPUIS, DEREK L	

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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/692,921
Filing Date: October 24, 2003
Appellant(s): JOHNSON ET AL.

Leopold Presser (Reg. No. 19,827)
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 3/20/2006 appealing from the Office action mailed 11/16/2005.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

No amendment after final has been filed.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

No evidence is relied upon by the examiner in the rejection of the claims under appeal.

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claims 1, 8, 11, and 18 are rejected under 35 U.S.C. 102(e) as being anticipated by ***Towle et al (US 6,834,133 B1)***.

Towle et al teach an optoelectronic packaging and method of packaging as shown in figures 1 and 2. Towle et al teach a substrate (122) bearing a first surface and a first cladding layer (120) positioned on the first surface of the substrate (122). A contact pad (124) is positioned on a portion of the surface of the first cladding layer (120) and a second cladding layer including a waveguide channel (112) is positioned on a further surface portion of the first cladding layer (120). The package also includes an optical means (116) that is in optical communication with the waveguide channel (112) and is in electrical contact with the contact pad (124) as is shown in the figures. The optical element is mounted on a transmitter/receiver chip (114) that is coupled to the second cladding layer (112). Towle et al teach that the transmitter/receiver chip is flip chip bonded to the waveguide and contact pad (see column 3, line 44 to column 5, line 9). Flip chip bonding involves the use of C4 joints as is well known in the semiconductor art.

Claims 2, 9, 10, 12, 19, and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over ***Towle et al (US 6,834,133 B1)*** as applied to claims 1, 8, 11, and 18 above, and further in view of ***Oono et al (US 2005/0105860 A1)***.

Towle et al teaches that the optoelectronic packaging is an PCB or an optoelectronic card used to align a waveguide and an optoelectronic device. However, Towle et al does not explicitly state that the optoelectronic device is a VCSEL. Towle et al also does not teach that the cladding layers are organic. Oono et al teach an optoelectronic device that couples a VCSEL (15) to an optical waveguide (112) as shown in the figures. Oono et al also teaches to use organic materials in claddings (see paragraph 171).

It would have been obvious to one of ordinary skill in the art at the time of invention to use a VCSEL as taught by Oono et al and to use an organic material as a cladding as taught by Oono et al in the optoelectronic package taught by Towle et al. Motivation to do this is that VCSEL emit light signals in a very defined direction thus making them more efficient in coupling light. Motivation to use an organic material would be that organic materials are known in the art to be stronger and more durable than inorganic materials such as glass and silicia.

Claims 5-7 and 15-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over ***Towle et al (US 6,834,133 B1)*** as applied to claims 1, 8, 11, and 18 above, and further in view of ***Yoshizawa et al (US 2002/0084522 A1)***.

Towle et al teaches that an optical solder is used to couple light between the emitter and the waveguide. Towle et al teaches that the solder is optically transmissive in the same range as the waveguide. Towle et al do not teach that the substrate is made of a material consisting of either epoxy glass, thick yarns or a low-expansion s-glass with a CTE as low as 10ppm/degree so as to alleviate the strain at the C4 joints. Yoshizawa et al teach an optoelectronic package where the substrate is formed of a material having a low thermal expansion coefficient such as a glass-fiber epoxy resin that reduces the stress of the flip chip bond by reducing the difference between the CTE of the substrate and chip (see paragraph 21). Yoshizawa et al teaches that the CTE of the substrate can be as low as 10 ppm/degree (see paragraph 25).

It would have been obvious to one of ordinary skill in the art at the time of invention to form the substrate of the device taught by Towle et al out of a material such as a glass-fiber epoxy resin as taught by Yoshizawa et al. Motivation to do this would be to reduce stress by

reducing the difference in the thermal expansion between the semiconductor chip and the substrate (see paragraph 21).

(10) Response to Argument

A. Objections to Claims 1 and 11 due to informality.

In response to appellant's argument that the minor typographical error has no bearing on the patentability or the scope of the appealed claims, the examiner agrees. However, the objection still stands due to the informaility.

B. Rejection Under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 6,834,133 B1 (Towle, et al).

1. Claims 1 and 8

In response to appellant's argument that Towle et al fail to disclose "at least one transmitter/receiver chip being coupled to the surface of the second cladding layer," the examiner disagrees. As explained in paragraph 9 of the final rejection, Towle et al teach a transmitter/receiver chip (114) with active area (116) coupled to the surface of the second cladding layer of the waveguide (112). Towle et al further explain that optoelectronic chips such as that indicated by reference number 114 can be used as transmitters and/or receivers (see column 1, lines 15-34). The waveguide (112) includes a core and a cladding since all waveguides include a core section surrounded by a cladding section so as to confine light within the core. While Towle et al use reference number (112) to refer to the entire waveguide structure, a core and a cladding layer are present in the waveguide, since this is the understood structure of an optical waveguide.

In pages 5-7, the appellant argues that Towle et al fail to disclose that "the at least one transmitter/receiver chip is coupled to the surface of the second cladding layer through the interposition of C-4 joints." The examiner disagrees with this assertion. As explained in paragraph 9 of the final rejection, Towle et al teach that the chip is "flip-chip bonded" to the waveguide and contact pad (see column 3, line 44 to column 5, line 9) and the flip-chip bonding structure involves the use of C-4 joints. The appellant defines C-4 joints in paragraph 20 of the disclosure. Appellant states that "a precise and passive alignment of VCSELs and receiver chips relative to the opto-electronic card (or printed circuit board) may be attained by means of a C4 solder reflow. Thus, it is well known in the technology that the surface tension of molten solder aligns the chips to the solder pads on the card or printed circuit board." The examiner maintains the position that convention flip chip bonded as described by Towle et al involves the use of C-4 joints. Further evidence of this would be that the flip chip bonding process taught by Towle et al clearly describes C-4 solder joints. While it does not explicitly say "C-4," it is clearly evident that the limitations of C-4 joints are described. Specifically, Towle et al teach that "during the bonding process, melting and hardening the solder bumps (126, 128) tends to draw the flip-chip (114) and the substrate (110) together in alignment due to a surface tension of the molten solder bumps 126 and 128. This process of alignment may be referred to as solder self-alignment." See column 4, lines 47-52. This process meets the definition of C-4 solder reflow given by the appellant in the disclosure. It is the through the interposition of the C-4 joints that the chip (114) is aligned with the waveguide (112).

2. Claims 11 and 18.

In page 7, the appellant argues that the rejection of claims 11 and 18 as being anticipated by Towle et al under 35 U.S.C. 102(e) is improper for the same reasons cited with regard to claims 1 and 8. The examiner disagrees with this assertion as discussed in the section above regarding claims 1 and 8.

C. Rejection Under 35 U.S.C. 103(a), as being unpatentable over Towle, et al. in view of Oono, et al.

1. Claims 2, 9, 10, 12, 19, and 20

Appellant argues that Oono et al fail to cure the alleged deficiencies of Towle et al with regard to claims 1, 8, 11, and 18. The examiner disagrees with this assertion. In the section above regarding claims 1, 8, 11, and 19, the examiner has explained how Towle et al teaches the claimed invention in claims 1, 8, 11, and 18.

Appellant further argues in page 7 that one of ordinary skill in the art would not combine the connections disclosed in Oono with "the novel features set forth in the present claims." The teachings of Oono are combined with the teachings of Towle et al, not the teachings of the appellant. Appellant further argues that one of ordinary skill in the art would not be motivated to combine the teachings of Towle et with the teachings of Oono et al. The rejection cited motivation to combine as discussed in paragraph 13 of the final rejection.

D. Rejection under 35 U.S.C. 103(a) as being unpatentable over Towle, et al. in view of Yoshizawa et al.

1. Claims 5-7 and 15-17

Appellant argues that Yoshizawa et al fail to cure the alleged deficiencies of Towle et al with regard to claims 1, 8, 11, and 18. The examiner disagrees with this assertion. In the section

above regarding claims 1, 8, 11, and 19, the examiner has explained how Towle et al teaches the claimed invention in claims 1, 8, 11, and 18.

Appellant further argues in pages 8 and 9 that neither Towle et al nor Yoshizawa et al disclose "low expansion materials to minimize strains in C-4 joints, as in claims 5, 6, 15, and 16, and the index-matched adhesive, as claimed in claims 7 and 17. The examiner disagrees with this assertion. As discussed in paragraph 15 of the final rejection, Yoshizawa et al teach an optoelectronic package where the substrate is formed of a material having a low thermal expansion coefficient such as a glass-fiber epoxy resin that reduces the stress of the flip chip bond by reducing the different between the CTE of the substrate and the chip (see paragraph 21 of Yoshizawa. As discussed above, the joints of conventional flip chip bonded chips are C-4 joints. Therefore, minimizing stress of flip chip bonds is minimizing stress on the C-4 joints.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

Derek L. Dupuis

Conferees:

Frank Font

Ricky Mack

Scully, Scott, Murphy & Presser, P.C.
400 Garden City Plaza – Suite 300
Garden City, New York 11530
(516) 742-4343